TRANSMISSION LINE STRUCTURE AND METHOD OF SIGNAL PROPAGATION

Background

For transmission line structures, propagation delay corresponds to the amount of time required for a signal to propagate its length. Manufactures of computers, integrated circuits, memories and other electrical circuits continually strive to reduce propagation delays in order to improve system operating speeds.

In the past, manufactures have been working to reduce circuit geometries, which has had the effect of improving operating speeds by way of reduced line lengths. More recently, however, manufactures are looking for additional means to improve operating speed. Such measures have included, e.g., lowering the resistance of conductive lines to reduce their RC delays.

In short, there have been continued efforts to provide computers, CPU's, semiconductor memories, integrated circuits, circuit boards, buses and other electrical devices structures and circuits to propagate signals quickly.

Brief Description of the Drawings

The present disclosure may be best understood with reference to the accompanying drawings, wherein:

FIG. 1 is a simplified cross sectional isometric view of an exemplary known transmission line structure;

FIG. 2 is a cross sectional view representative of the transmission line structure in accordance with an exemplary embodiment of the present invention;

FIG. 3 is a partial cross sectional isometric view of the transmission line structure in accordance with an exemplary embodiment of the present invention;

FIG. 4 is a cross sectional view of the transmission line structure in accordance with another exemplary embodiment of the present invention, in which dielectric is formed over and between the lines;

FIG. 5 is a schematic diagram representative of the transmission line circuit in accordance with an exemplary embodiment of the present invention; and

FIG. 6 is a simplified block diagram representative of exemplary embodiments of the present invention showing a computer system with transmission line structures for at least one of the processor, bus or an associated integrated circuit.

Detailed Description

In the following description, numerous specific details are set forth to provide an understanding of the present invention. However, it will be understood that the present invention may be practiced without each of such specific details. In other instances, well-known circuits are shown in block diagram form in order to prevent obscuring the present invention with unnecessary detail. For the most part, detailed particulars concerning timing considerations and the like are omitted inasmuch as such details are not necessary to obtain a complete understanding of the present invention and are within the ability of persons of ordinary skill in the relevant art.

In the drawings , elements are not necessarily drawn to scale. Additionally, like or similar elements are typically designated by the same number through the separate views.

Referencing FIG. 1, an exemplary known transmission line structure for an integrated circuit comprises microstrip 10. Such microstrip comprises conductor 18 disposed over a surface of dielectric 14 opposite conductive layer 16. Such exemplary transmission lines might also include dielectric -- e.g., Spin On Glass, BPSG, nitride, polyimide (not shown) -- over conductor 18 and substrate 12.

Further referencing FIG. 1, different qualities characterize transmission line 10. Its characteristic impedance may be determined in known manner based upon the width of conductor 18, in addition to its thickness, distance from conductive layer 16 (e.g., ground plane) and the relative dielectric constant ϵ_r of dielectric 14. Another quality is its propagation delay, the time T required for a signal to propagate along its length l. The propagation delay of transmission line 10 is affected by its phase velocity v_p, which is modeled by the following equation.

$$T = \frac{l}{v_p} \qquad \textbf{Equation 1}$$

For an inhomogeneous transmission line, i.e., of non-uniform dielectric environment, the phase velocity is defined as being related to the velocity of light c divided by the effective dielectric constant ϵ_{eff} of the line, as shown by the equation below.

$$Vp = \frac{c}{\sqrt{E_{eff}}}$$ **Equation 2**

The effective dielectric constant E_{eff}, in turn, is related to the capacitance C of the line divided by its linear capacitance C_o:

$$E_{eff} = \frac{C}{C_o}$$ **Equation 3**

in which the linear capacitance C_o represents the line capacitance with the dielectric 14 replaced with air.

It has been found, in accordance with an exemplary embodiment of the present invention, that propagation delays of integrated circuits may be improved with new transmission line circuits.

With reference to FIGS. 2-3, in accordance with an exemplary embodiment of the present invention, conductive lines 22 over surface 15 of dielectric 14 define structure 20 for propagating a signal across substrate 12. In the illustrated example, three conductive lines 24,26,28 may be patterned across surface 15 of substrate 12. The height h of the conductive lines may be established by the distance of their top wall 36 relative to their bottom wall (or edge) 34 over dielectric 15. Side walls 30,31 of adjacent conductive lines face one another to define gap 38. In this embodiment, two outer conductive lines 24,28 sandwich a center conductive line 26 and define a gap spacing therebetween. The gap spacing may be less than the height *h* of the conductive lines. In alternative embodiments, the conductive lines may be formed to define the gap with a distance less than two-thirds the height of the conductive lines – i.e., $S \le 2h/3$. Relative to the cross-section of FIG. 2, this corresponds to a gap aspect ratio greater than 1.5:1.

In some embodiments, the height *h* of the conductive lines may be designed to be greater than the gap distance *s*. It has been found that by keeping the height h of the conductive lines greater than the gap distance S, that advantages are observed in a speed of signal propagation along transmission line structure 20.

In accordance with an alternative exemplary embodiment of the present invention, the intercoupling capacitance from the center line 26 to the outer lines 24,28 may be kept greater then the capacitance of the center line 26 to conductive layer (e.g., ground plane) 16 through dielectric 14.

Referencing FIG. 4, each of transmission lines 24,26,28 comprises a capacitance (i.e., per unit length) to ground of C_B,C_A,C_C respectively, where C_A represents the capacitance of the center conductive line 26 to ground. Additionally, the center conductive line 26 comprises cross capacitances C_{AB} and C_{AC} to the adjacent outer conductive lines 24,28 respectively. A resistance per unit length R_B, R_A, R_C of the conductive lines may be established based upon their material composition.

In accordance with an exemplary embodiment of the present invention, the ratio of the capacitances C_{AB} and C_{AC} to the adjacent lines may be kept at least equal to the capacitance C_A of the center line to ground.

In accordance with a particular exemplary embodiment of the present invention, the transmission line structure may be formed over an integrated circuit comprising a layer of silicon oxide dielectric. From the above relationships, ignoring fringing fields, the capacitance (per unit length) C_A can be expressed as equal to the width W of the line multiplied by the dielectric constant $\epsilon_r \epsilon_o$, divided by the thickness t of the dielectric.

$$C_A = \frac{E_r E_o W}{t} \qquad \textbf{Equation 4}$$

For the capacitance couplings to the adjacent conductive lines, the capacitances (per unit length) C_{AB}, C_{AC} are expressed as being equal to their height h multiplied by the free space permittivity (i.e., ϵ_o) divided by the gap spacing s.

$$C_{AB} = \frac{E_o h}{s} \qquad \textbf{Equation 5}$$

In accordance with this particular exemplary embodiment, the capacitances C_{AB}+C_{AC} to the adjacent lines may be kept at least as large as the line's capacitance C_A to ground. Accordingly, the relationship

$$\frac{E_o h}{s} \geq \frac{E_r E_o W}{2t} \qquad \textbf{Equation 6}$$

leading to

$$\frac{h}{s} \geq \frac{E_r W}{2t} \qquad \textbf{Equation 7}$$

In accordance with another exemplary embodiment of the present invention, referencing FIG. 5, dielectric 13 may be provided over and between the lines. In a particular exemplary embodiment, the dielectric may comprise material the same as the

dielectric 14 beneath the conductive lines. Relative to Equation 6, the left term picks-up an additional multiplier ϵ_r, and the resultant relationship may be expressed by Equation 8 as follows:

$$\frac{h}{s} \geq \frac{W}{2t} \qquad \textbf{Equation 8}$$

The *h/s* ration of the conductive lines, in accordance with this embodiment, may be kept at least as large as *W/2t*, i.e., one-half the ratio of the width *W* of the conductive lines relative to their thickness *t* of the underlying dielectric thickness. It is believed, pursuant this exemplary embodiment, that the neighboring outside conductive lines driven with the same signal may expedite propagation of the signal along the middle conductive line.

In accordance with alternative embodiments, further referencing FIG. 5, the additional dielectric 13 may comprise a surface 17 approximately level with the conductive lines. In other embodiments, although not shown, the upper surface of dielectric 13 may not be level with the height of the conductive lines.

In FIGS. 3 and 5, substrate 12 is shown as comprising simply dielectric 14 over conductive layer (e.g., ground plane) 16. Alternatively, substrate 12 may comprise further supporting layers, or other portions of semiconductor structures. Such other portions are not shown herein for purposes of simplifying the present disclosure. It is understood, however, that the scope of the present invention encompasses such alternative substrates.

Additionally, the dielectric 14 and ground plane 16 of FIGS. 3 and 5 are shown in simplified fashion as comprising planar level structures. In alternative embodiments of the present invention, the conductive lines may traverse a non-planar (not shown) surface. For example, the substrate may be formed with a groove, wherein the lines may traverse the groove contour. Alternatively, the conductive lines may be supported with edges coupled to a surface of a dielectric sidewall (not shown) that defines at least in part a groove within the substrate.

In accordance with further exemplary embodiments, referencing FIG. 4, the plurality of conductive lines 24,26,28 of the transmission line structure 20 may be configured to receive a common signal. As shown in FIG. 4, again, the plurality of conductive lines 24,26,28 may be represented schematically as distributed resistors 48,

inter-coupling capacitors 52 and shunt capacitors 50. In this embodiment, at an input side 43 of each of the conductive lines, drivers 42 drive respective source terminals of the lines of the plurality. Line driver 42A is coupled to the input node 43A of the center conductive line 26, while line drivers 42B,42C are coupled to input nodes 43B,43C of the outer conductive lines 24,28 respectively. The drivers, may present the same source impedance to each of the conductive lines. The driver inputs receive a common signal from signal node 46.

In accordance with an exemplary embodiment, driver outputs may meet the conductive lines at positions 43 proximate one another. In other words, the drivers 42B,42C meet input terminals 43B,43C of the conductive line at substantially the same positions over the substrate as that by which line driver 42A meets input terminal 43A of conductive line 26.

Further referencing FIG. 4, the drivers 42 receive data signals from data buffer 44. Data buffer may receive a data signal from, e.g., one of a processor, memory device, keyboard, terminal, router, bus controller or other device. To keep within the pitch of the conductive lines, the line drivers 42 may be kept separate, allowing for smaller geometry designs of lower drive requirements. Additionally, any return reflections of a particular line may be kept isolated (via the separate drivers) from the common signal node 46, and likewise isolated from the center conductive line 26. Further, external noise may be shielded form the center conductor 26 by outer conductive lines 24,28.

On the output side, the center conductor 26 may be coupled to forward the propagated signal to the output destination. For example, as shown in FIG. 4, the center conductor 26 may be coupled to data receiver 56 at an output terminal. Data receive 56 may receive and buffer the propagated signal for other uses. Dummy loads 61,62 may be coupled to the output terminals 54B,54C to terminate signals propagated thereby. In this embodiment, the dummy loads may meet the respective outer conductive lines 24,28 at positions proximate the coupling position of data receiver 56 relative to the center conductive line 26. As shown in FIG. 4, the dummy loads comprise receivers similar to data receiver 56, which is coupled to center conductive line 26. Alternatively, the dummy loads may comprise simple resistors shorted to ground. Further, data receiver 56 and dummy loads 61,62 may present similar matching impedances to the output terminals of their respective lines.

Referencing FIG. 6, in accordance with another exemplary embodiment of the present invention, a processor system 70 comprises processor 72 coupled to bus 74. Bus 74 is coupled to a plurality of sub-systems of the processor system 70, including, e.g., a keyboard, mouse, microphone, monitor, sampler interface, network interface card, printer, disk storage and/or the like 76. Additionally, bus 74 interfaces memory module 78. Memory module 78 comprises memory 80 operable under the control of a controller.

In accordance with a more particular exemplary embodiment, processor 72 comprises a transmission line structure 120 of an exemplary embodiment previously disclosed herein relative to FIGS. 3-5 over a substrate 112. In accordance with a further exemplary embodiment, memory device 80, e.g., of a semiconductor integrated circuit, likewise comprises a transmission line structure 220 as associated with an exemplary embodiment previously disclosed herein relative to FIGS. 3-5 over an insulating layer of substrate 212. In yet a further exemplary embodiment, bus 74 of the computer system might also employ a transmission line structure 320 over a substrate 312 per an exemplary embodiment disclosed previously herein relative to FIGS. 3-5.

It will be apparent to those skilled in this art that the illustrated embodiments are exemplary and that various changes and modifications may be made thereto as become apparent upon reading the present disclosure. Accordingly, such changes and modifications are considered to fall within the scope of the appended claims.